REMARKS

Examiner L. Umez-Eronini is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 6, 11, 16, 21, and 26 have been amended.

Reconsideration of the rejection of Claims 1, 6, 11, 16, 21, and 26 under 35 U.S.C. 112, first paragraph, is respectfully requested. It is believed that the limitation "wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer" is fully supported by the Specification and drawings. Specifically, it is stated on the top of page 6 that an etch stop/barrier layer is not required in the process of the invention. The absence of an etch stop layer is one of the objects of the invention, stated in the third paragraph of page 3 of the Specification. For example, the second paragraph of page 9 states that no etch stop layer was used in the process of the invention.

Claim 21 has been amended to overcome rejection under 35 U.S.C. 112. Claim 6 had the same error in wording. The Examiner is thanked for noticing this error. All Claims are believed to be in condition for Allowance and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1, 3, and 5 as being unpatentable over Chow in view of Toshiaki and further in view of Kudo is requested in view of Amended Claim 1 and in accordance with the following remarks.

Claim 1 details a via-first dual damascene method as shown in Figs. 1-7. The key feature of Applicants' invention is that no high dielectric constant material is required as an etch stop or barrier layer (see page 6 of the Specification). Chow shows the use of etch stop layers. It is agreed that Toshiaki lacks an etch stop layer, but Toshiaki requires a topmost inorganic layer 4 in addition to the inorganic layer 2 and organic layer 3. The inorganic layer 4 acts as a hard mask. THus, it is agreed with the Examiner that Chow in view of Toshiaki does not teach using patterned inorganic dielectric layer as a mask.

It is agreed that Kudo et al teaches using an inorganic film as a mask (col. 14, lines 34-41). This relates to Fig. 8J. Moving on in that process, another photoresist pattern is formed for the wiring trench and that is etched into the organic film 62 using the inorganic film 63 as a hard mask as shown in FIg. 8K (col. 14, lines 42-53). However, the via and trench are both formed in the single organic film 62. This differs from Applicants' invention where the via is

formed in the organic layer and the trench is formed in the inorganic layer (see Fig. 6 and Claim 1). Claim 1 has been amended to make it clear that the organic dielectric layer acts as an etch stop when the trench is etched into the inorganic dielectric layer. It is believed that the combination of references does not teach or suggest the detailed now claimed process of Applicant's invention where only two dielectric layers are employed to form the via and trench in a via-first process without an additional etch stop layer.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1, 3, and 5 as being unpatentable over Chow in view of Toshiaki and further in view of Kudo is requested in view of Amended Claim 1 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 2 as being unpatentable over Chow in view of Toshiaki and Kudo and further in view of Joshi et al is requested in view of Amended Claim 1 and in accordance with the following remarks.

It is agreed that Joshi et al teaches forming semiconductor devices wherein metal lines overlie the devices. However, it is believed that the amendment to

Claim 1 makes it clear that the key feature of Applicants' invention not taught in the prior art is a via first dual damascene process without an etch stop layer between the two low-k dielectric layers where the via is formed in the first dielectric layer and the trench is formed within the second dielectric layer.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 2 as being unpatentable over Chow in view of Toshiaki and Kudo and further in view of Joshi et al is requested in view of Amended Claim 1 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 4 as being unpatentable over Chow in view of Toshiaki and Kudo and further in view of Wang et al is requested in view of Amended Claim 1 and in accordance with the following remarks.

It is agreed that Wang et al teaches forming a dielectric layer that can comprise silicon dioxide or another material such as FSG. However, this layer is used as an etch stop layer in etching an overlying nitride layer (col. 6, lines 65-67) and then as a hard mask for etching the underlying metal layer (col. 8, lines 20-29). This has

nothing to do with the low-k dielectric layer of Applicants' invention through which a dual damascene opening is made. Furthermore, it is believed that the amendment to Claim 1 makes it clear that the key feature of Applicants' invention not taught in the prior art is a via first dual damascene process without an etch stop layer between the two low-k dielectric layers where the via is formed in the first dielectric layer and the trench is formed within the second dielectric layer.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 4 as being unpatentable over Chow in view of Toshiaki and Kuo et al and further in view of Wang et al is requested in view of Amended Claim 1 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 8, and 10 as being unpatentable over Chow in view of Toshiaki is requested in view of Amended Claim 6 and in accordance with the following remarks.

Claim 6 details a trench-first dual damascene method as shown in Figs. 8-13. The key feature of Applicants' invention is that no high dielectric constant material is required as an etch stop or barrier layer (see page 6 of the

Specification). Chow shows the use of an etch stop layer and does not disclose a trench-first process. Toshiaki shows a process without an etch stop layer, but requires three dielectric layers in order to form the dual damascene opening. The topmost inorganic layer acts as a hard mask. Toshiaki teaches a via first process rather than a trench first process. If the Examiner takes the position that etching the trench opening in layer 4 is a trench-first process (see Fig. 5 and paragraph 0014), then additional steps are required in Toshiaki. After the via is patterned (FIg. 7 and paragraph 0015), the trench must be etched into the layer 3 (see Fig. 8 and paragraph 0016). Applicants' use only two dielectric layers to form their trench and via in the trench-first process taught in Claim 6.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 8, and 10 as being unpatentable over Chow in view of Toshiaki is requested in view of Amended Claim 6 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 7 as being unpatentable over Chow in view of Toshiaki and further in view of Joshi et al is requested in view of Amended Claim 6 and in accordance with the following remarks.

It is agreed that Joshi et al teaches forming semiconductor devices wherein metal lines overlie the devices. However, none of the references teach a trench-first process. Applicants' use only two dielectric layers to form their trench and via in the trench-first process taught in Claim 6. This process is not taught or suggested by the references.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 7 as being unpatentable over Chow in view of Toshiaki further in view of Joshi et al is requested in view of Amended Claim 6 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 9 as being unpatentable over Chow in view of Toshiaki and further in view of Wang et al is requested in view of Amended Claim 6 and in accordance with the following remarks.

As discussed above, it is agreed that Wang et al teaches forming a dielectric layer that can comprise silicon dioxide or another material such as FSG. However, this layer is used as an etch stop layer in etching an overlying nitride layer (col. 6, lines 65-67) and then as a hard mask for etching the underlying metal layer (col. 8, lines 20-29). This has nothing to do with the low-k dielectric layer of Applicants'

invention through which a dual damascene opening is made. Furthermore, none of the references teach a trench-first process. Applicants' use only two dielectric layers to form their trench and via in the trench-first process taught in Claim 6. This process is not taught or suggested by the references.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 9 as being unpatentable over Chow in view of Toshiaki and further in view of Wang et al is requested in view of Amended Claim 6 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 11, 13, and 15 as being unpatentable over Chow in view of Toshiaki is requested in view of Amended Claim 11 and in accordance with the following remarks.

Claim 11 details a self-aligned dual damascene method as shown in Figs. 14-19. The key feature of Applicants' invention is that no high dielectric constant material is required as an etch stop or barrier layer (see page 6 of the Specification). Chow shows the use of etch stop layers and does not teach a self-aligned method. Toshiaki does show a method where an etch stop layer is not used, but also does not teach a self-aligned method. Claim 11 has been amended

to state that two different etching recipes are used during the etching of the via pattern and the trench pattern since the two layer materials are different. This is disclosed in the Specification in the paragraph bridging pages 14 and 15. This self-aligned method with differing etching recipes is not taught or suggested by the references.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 11, 13, and 15 as being unpatentable over Chow in view of Toshiaki is requested in view of Amended Claim 11 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 12 as being unpatentable over Chow in view of Toshiaki and further in view of Joshi et al is requested in view of Amended Claim 11 and in accordance with the following remarks.

It is agreed that Joshi et al teaches forming semiconductor devices wherein metal lines overlie the devices. However, it is believed that the amendment to Claim 11 makes clear Applicants' self-aligned method with differing etching recipes which is not taught or suggested by the references.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 12 as being unpatentable over Chow in view of Toshiaki and further in view of Joshi et al is requested in view of Amended Claim 11 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 14 as being unpatentable over Chow in view of Toshiaki and further in view of Wang et al is requested in view of Amended Claim 11 and in accordance with the following remarks.

As discussed above, it is agreed that Wang et al teaches forming a dielectric layer that can comprise silicon dioxide or another material such as FSG. However, this layer is used as an etch stop layer in etching an overlying nitride layer (col. 6, lines 65-67) and then as a hard mask for etching the underlying metal layer (col. 8, lines 20-29). This has nothing to do with the low-k dielectric layer of Applicants' invention through which a dual damascene opening is made. Furthermore, it is believed that the amendment to Claim 11 makes clear Applicants' self-aligned method with differing etching recipes which is not taught or suggested by the references.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 14 as being unpatentable over Chow in view of Toshiaki and further in view of Wang et al is requested in view of Amended Claim 11 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 16, 19, and 20 as being unpatentable over Chow in view of Toshiaki is requested in view of Amended Claim 16 and in accordance with the following remarks.

Claim 16 details a via-first dual damascene method as shown in Figs. 1-7. The key feature of Applicants' invention is that no high dielectric constant material is required as an etch stop or barrier layer (see page 6 of the Specification). Chow shows the use of etch stop layers. It is agreed that Toshiaki lacks an etch stop layer, but Toshiaki requires a topmost inorganic layer 4 in addition to the inorganic layer 2 and organic layer 3. The inorganic layer 4 acts as a hard mask. Thus, Chow in view of Toshiaki does not teach using the patterned organic dielectric layer as a mask (Claim 16, lines 14-16). Claim 16 has been amended to make it clear that the inorganic dielectric layer acts as an etch stop when the trench is etched into the inorganic dielectric layer. This is not taught or suggested by either of the references.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 16, 19, and 20 as being unpatentable over Chow in view of Toshiaki is requested in view of Amended Claim 16 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 17 as being unpatentable over Chow in view of Toshiaki and further in view of Joshi et al is requested in view of Amended Claim 16 and in accordance with the following remarks.

It is agreed that Joshi et al teaches forming semiconductor devices wherein metal lines overlie the devices. However, it is believed that the amendment to Claim 16 makes it clear that the key feature of Applicants' invention not taught in the prior art is a via first dual damascene process without an etch stop layer between the two low-k dielectric layers where the via is formed in the first dielectric layer and the trench is formed within the second dielectric layer and wherein the bottom layer acts as an etch stop when the trench is etched into the top layer.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 17 as being unpatentable over Chow in view of Toshiaki and further in view of Joshi et al is requested in view of

Amended Claim 16 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 18 as being unpatentable over Chow in view of Toshiaki and further in view of Wang et al is requested in view of Amended Claim 16 and in accordance with the following remarks.

It is agreed that Wang et al teaches forming a dielectric layer that can comprise silicon dioxide or another material such as FSG. However, this layer is used as an etch stop layer in etching an overlying nitride layer (col. 6, lines 65-67) and then as a hard mask for etching the underlying metal layer (col. 8, lines 20-29). This has nothing to do with the low-k dielectric layer of Applicants' invention through which a dual damascene opening is made. Furthermore, it is believed that the amendment to Claim 16 makes it clear that the key feature of Applicants' invention not taught in the prior art is a via first dual damascene process without an etch stop layer between the two low-k dielectric layers where the via is formed in the first dielectric layer and the trench is formed within the second dielectric layer and wherein the bottom layer acts as an etch stop when the trench is etched into the top layer.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 18 as being unpatentable over Chow in view of Toshiaki and further in view of Wang et al is requested in view of Amended Claim 16 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 21, 24, and 25 as being unpatentable over Chow in view of Toshiaki is requested in view of Amended Claim 21 and in accordance with the following remarks.

Claim 21 details a trench-first dual damascene method as shown in Figs. 8-13. The key feature of Applicants' invention is that no high dielectric constant material is required as an etch stop or barrier layer (see page 6 of the Specification). Chow shows the use of an etch stop layer and does not disclose a trench-first process. Toshiaki shows a process without an etch stop layer, but requires three dielectric layers in order to form the dual damascene opening. The topmost inorganic layer acts as a hard mask. Toshiaki teaches a via first process rather than a trench first process. If the Examiner takes the position that etching the trench opening in layer 4 is a trench-first process (see Fig. 5 and paragraph 0014), then additional steps are required in Toshiaki. After the via is patterned (FIg. 7 and paragraph 0015), the trench must be etched into

the layer 3 (see Fig. 8 and paragraph 0016). Applicants use only two dielectric layers to form their trench and via in the trench-first process taught in Claim 21.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 21, 24, and 25 as being unpatentable over Chow in view of Toshiaki is requested in view of Amended Claim 21 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 26 and 29 as being unpatentable over Chow in view of Toshiaki and further in view of Joshi et al is requested in view of Amended Claim 6 and in accordance with the following remarks.

Claim 26 details a self-aligned dual damascene method as shown in Figs. 14-19. The key feature of Applicants' invention is that no high dielectric constant material is required as an etch stop or barrier layer (see page 6 of the Specification). Chow shows the use of etch stop layers and does not teach a self-aligned method. Toshiaki does show a method where an etch stop layer is not used, but also does not teach a self-aligned method. Claim 26 has been amended to state that two different etching recipes are used during the etching of the via pattern and the trench pattern since

the two layer materials are different. This is disclosed in the Specification in the paragraph bridging pages 14 and 15. This self-aligned method with differing etching recipes is not taught or suggested by the references.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 26 and 29 as being unpatentable over Chow in view of Toshiaki is requested in view of Amended Claim 26 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 27 as being unpatentable over Chow in view of Toshiaki and further in view of Joshi et al is requested in view of Amended Claim 26 and in accordance with the following remarks.

It is agreed that Joshi et al teaches forming semiconductor devices wherein metal lines overlie the devices. However, it is believed that the amendment to Claim 26 makes clear Applicants' self-aligned method with differing etching recipes which is not taught or suggested by the references.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 27 as being unpatentable over Chow in view of Toshiaki

and further in view of Joshi et al is requested in view of Amended Claim 26 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 28 as being unpatentable over Chow in view of Toshiaki and further in view of Wang et al is requested in view of Amended Claim 26 and in accordance with the following remarks.

As discussed above, it is agreed that Wang et al teaches forming a dielectric layer that can comprise silicon dioxide or another material such as FSG. However, this layer is used as an etch stop layer in etching an overlying nitride layer (col. 6, lines 65-67) and then as a hard mask for etching the underlying metal layer (col. 8, lines 20-29). This has nothing to do with the low-k dielectric layer of Applicants' invention through which a dual damascene opening is made. Furthermore, it is believed that the amendment to Claim 26 makes clear Applicants' self-aligned method with differing etching recipes which is not taught or suggested by the references.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 28 as being unpatentable over Chow in view of Toshiaki and further in view of Wang et al is requested in view of

Amended Claim 26 and in accordance with the remarks above.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner Umez-Eronini not find that the Claims are now Allowable that she call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

Rosemary L. S. Pike. Reg # 39,332

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the Claims as follows:

1. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a via pattern into said inorganic dielectric layer;

etching said via pattern into said organic dielectric layer using patterned said inorganic dielectric layer as a mask; and

thereafter etching a trench pattern into said inorganic dielectric layer <u>wherein said organic dielectric layer acts as an etch stop</u> to complete said

forming of said dual damascene openings in the fabrication of said integrated circuit device.

6. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a trench pattern into said inorganic dielectric layer; and

thereafter etching a via pattern [through said inorganic dielectric layer and] <u>into</u> said organic dielectric layer <u>through said trench pattern</u> to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

11. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a via pattern into said inorganic dielectric layer; and

simultaneously etching said via pattern into said organic dielectric layer and etching a trench pattern into said inorganic dielectric layer wherein one etching recipe is used for said organic dielectric layer and a different etching recipe is used for said inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

16. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an inorganic dielectric layer overlying

said insulating layer;

depositing an organic dielectric layer overlying said inorganic dielectric layer wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric layer;

etching a via pattern into said organic dielectric layer;

etching said via pattern into said inorganic dielectric layer using patterned said organic dielectric layer as a mask; and

thereafter etching a trench pattern into said organic dielectric layer wherein said inorganic dielectric layer acts as an etch stop to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

21. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an inorganic dielectric layer overlying said insulating layer;

depositing an organic dielectric layer overlying said inorganic dielectric layer wherein no etch stop

layer is formed between said inorganic dielectric layer and said organic dielectric layer;

etching a trench pattern into said organic dielectric layer; and

thereafter etching a via pattern [through said organic dielectric layer and] <u>into</u> said inorganic dielectric layer <u>through said trench pattern</u> to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

26. (TWICE AMENDED) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an inorganic dielectric layer overlying said insulating layer;

depositing an organic dielectric layer overlying said inorganic dielectric layer wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric layer;

etching a via pattern into said organic dielectric layer; and

simultaneously etching said via pattern into said inorganic dielectric layer and etching a trench pattern

into said organic dielectric layer to wherein one etching recipe is used for said organic dielectric layer and a different etching recipe is used for said inorganic dielectric layer complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.